* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] silicon substrate top the compound semiconductor substrate made [the group-III-V-semiconducter layer] to carry out epitaxial growth -- setting -- the above it consists of the same configuration element as a group-III-V-semiconducter layer -- compared with an III group atom, V group atom is superfluously included in 1.5% or less of range 0.2% or more Compound semiconductor substrate characterized by including at least one or more layers of group-III-V-semiconducter layers.
[Claim 2] silicon substrate top a group-III-V-semiconducter layer is set to the manufacture approach of the compound semiconductor substrate which carries out epitaxial growth -- V group atom is made to incorporate superfluously in 1.5% or less of range 0.2% or more compared with an III group atom, and V group atom is included superfluously The manufacture approach of the compound semiconductor substrate characterized by including the process into which a group-III-V-semiconducter layer is grown up.
[Claim 3] Compared with an III group atom, V group atom is included superfluously. After carrying out epitaxial growth of the group-III-V-semiconducter layer, it is made to grow up after that. The manufacture approach of the compound semiconductor substrate according to claim 2 characterized by giving the heat treatment process in temperature higher than the growth temperature of a group-III-V-semiconducter layer.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the compound semiconductor substrate used for light or a high-speed electron device by the detail, and its manufacture approach more about a compound semiconductor substrate and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, epitaxial growth of the compound semiconductor of a different kind is carried out to this on a substrate, and the compound semiconductor substrate which can utilize each advantage in said substrate and compound semiconductor is studied. For example, by carrying out epitaxial growth of the GaAs on a silicon (it being hereafter described as Si) substrate, the compound semiconductor substrate which combines the mechanical strength which Si holds, and the high-speed responsibility which GaAs holds is produced, and the compound semiconductor substrate obtained by such approach is applied to the electron device, the optical device, etc. However, it is easy to spread said rearrangement with the stress which there was a big difference in the lattice constant and coefficient of thermal expansion in Si and GaAs, it originated in this lattice constant difference, and the rearrangement was [stress] easy to be formed in the interface of Si substrate and a GaAs layer, and was generated based on said coefficient-of-thermal-expansion difference toward the front face of said GaAs layer. Consequently, many said rearrangements existed in said GaAs layer front face, the crystallinity near [in said GaAs layer] the front face fell to it, and there was a problem that it was difficult to demonstrate the function as a device etc. good.
[0003] To insert the rearrangement reduction layer for controlling propagation of a rearrangement into said GaAs layer as an approach of reducing dislocation density [/ near the GaAs layer front face] is tried. The distorted superlattice layer which has a different presentation from a GaAs layer in this rearrangement reduction layer, the layer by which the impurity was added are examined (application physics: 61 No. 2 and pp(s) 126-133, and 1992).
[0004] The compound with which a lattice constant differs from GaAs layers, such as for example, an InGaAs layer and a GaAsP layer, is used for said distorted superlattice layer, if this distortion super-latticed layer is inserted, it will be distorted, the propagation of said rearrangement will be bent, and reduction of dislocation density [/ near / said / the GaAs layer front face] will be achieved by [which arose from now on] suppressing propagation of this rearrangement. Moreover, if impurities, such as Zn, In, and Si atom, are added in a GaAs layer, propagation of the rearrangement near [said] the GaAs layer front face will be controlled by the effectiveness that a crystal becomes hard, and the effectiveness that pinning of said rearrangement is carried out, and reduction of dislocation density will be achieved according to them.
[0005]
[Problem(s) to be Solved by the Invention] However, in the compound semiconductor substrate with which the above-mentioned distorted superlattice layer was inserted, the band structure of a GaAs layer tended to change with said distorted superlattice layers, and the technical problem that change of this

band structure tends to have a bad influence on the electrical characteristics near the GaAs layer front face occurred.
[0006] Moreover, in the compound semiconductor substrate with which said impurity was added, after said impurity was spread near the GaAs layer front face from said rearrangement reduction layer, impurities, such as Zn, In, or Si atom, acted as a dopant, and the technical problem that change arose to carrier concentration [/ near the GaAs layer front face], and it was easy to have a bad influence on electrical characteristics occurred.
[0007] It is made in view of such a technical problem, and this invention is on Si substrate. There is little dislocation density [/ near / the group-III-V-semiconducter layer was made to carry out epitaxial growth / the compound semiconductor substrate front face], and it also aims change of band structure or carrier concentration at offering the compound semiconductor substrate and its manufacture approach of little high quality excellent in electrical characteristics.
[0008]
[Means for Solving the Problem] the compound semiconductor substrate applied to this invention in order to attain the above-mentioned purpose -- silicon substrate top the compound semiconductor substrate made [the group-III-V-semiconducter layer] to carry out epitaxial growth -- setting -- the above it consists of the same configuration element as a group-III-V-semiconducter layer -- compared with an III group atom, V group atom is superfluously included in 1.5% or less of range 0.2% or more (1) characterized by including at least one or more layers of group-III-V-semiconducter layers.
[0009] moreover, the manufacture approach of the compound semiconductor substrate concerning this invention -- silicon substrate top a group-III-V-semiconducter layer is set to the manufacture approach of the compound semiconductor substrate which carries out epitaxial growth -- V group atom is made to incorporate superfluously in 1.5% or less of range 0.2% or more compared with an III group atom, and V group atom is included superfluously (2) characterized by including the process into which a group-III-V-semiconducter layer is grown up.
[0010] Moreover, the manufacture approach of the compound semiconductor substrate concerning this invention contains V group atom superfluously by the manufacture approach of the compound semiconductor substrate the above-mentioned (2) publication compared with an III group atom. After carrying out epitaxial growth of the group-III-V-semiconducter layer, it is made to grow up after that. It is characterized by giving the heat treatment process in temperature higher than the growth temperature of a group-III-V-semiconducter layer (3).
[0011]
[Function] For example, in the case of the GaAs (III-V group compound) layer, it is known by making it grow up at low-temperature (200-300 degrees C) predetermined temperature comparatively using a molecular-beam-epitaxy method that epitaxial growth of the GaAs layer which contains As (III group atom) of superfluous predetermined concentration compared with Ga (V group atom) can be carried out (Thin Solid Films:231 (1993) 61-73). In this case, the superfluous content concentration of As in said GaAs layer is controlled by mainly changing growth temperature.
[0012] It is the typical sectional view which drawing 6 showed in order to explain propagation of the rearrangement in the compound semiconductor substrate containing one layer of GaAs layers which a GaAs layer is made to carry out epitaxial growth on Si substrate, and contain As superfluously in this GaAs layer, and, as for 11 in drawing, Si substrate is shown. On the Si substrate 11, the GaAs layer 12 which carried out epitaxial growth is formed, and the GaAs layer 13 containing superfluous As is formed on the GaAs layer 12. Since the GaAs layer 13 is comparatively grown up at low-temperature predetermined temperature using the above-mentioned molecular-beam-epitaxy method and balking of As from GaAs layer 13 front face is controlled in the case of growth, superfluous As is incorporated by stoichiometric in the GaAs layer 13. Moreover, on the GaAs layer 13, the GaAs layer 14 which carried out epitaxial growth to the GaAs layer 12 like abbreviation is formed, a part of As superfluously incorporated in the GaAs layer 13 in the epitaxial growth process of the GaAs layer 14 will condense, and it will deposit as metal As13a.
[0013] Thus, in the constituted compound semiconductor substrate, pinning of the rearrangement 15

generated in the interface of the Si substrate 11 and the GaAs layer 12 will be carried out by metal As13a. Therefore, except for a part of rearrangement 15a, almost all the rearrangements 15 will be blocked by the GaAs layer 13, and the propagation to the GaAs layer 14 will be prevented, consequently the consistency of rearrangement 15a [/ near the GaAs layer 14 front face] decreases. While, as for the superfluous content of As in the GaAs layer 13 for decreasing the consistency of rearrangement 15a, 0.2% or more is needed, a upper limit will be restrained by the grown method and 1.5% becomes a upper limit in molecular beam epitaxy.

[0014] According to the compound semiconductor substrate (1) of the above-mentioned configuration, it describes above. Compared with an III group atom, said V group atom is superfluously included in 1.5% or less of range 0.2% or more. Said some of V group atoms may be made to condense and deposit in a group-III-V-semiconducter layer. By this condensation and V group atom particle which deposited The above which carried out epitaxial growth on Si substrate and this Si substrate Pinning of the rearrangement produced in the interface with a group-III-V-semiconducter layer can be carried out. For this reason, said V group atom is included superfluously. It describes above by the group-III-V-semiconducter layer. Propagation of the rearrangement to a group-III-V-semiconducter layer front face can be blocked, consequently it describes above. Dislocation density [/ near the group-III-V-semiconducter layer front face] can be reduced. Moreover, said V group atom is included superfluously. Since any atoms other than the configuration element of a compound semiconductor layer are not included in a group-III-V-semiconducter layer, it describes above. While being able to lessen effect affect the band structure of a group-III-V-semiconducter layer, the compound semiconductor substrate of the high quality which can also lessen change of carrier concentration, therefore was excellent in electrical characteristics will be obtained.

[0015] Moreover, the process which makes V group atom in the manufacture approach (2) of the compound semiconductor substrate of the above-mentioned configuration incorporate superfluously is easily carried out by adopting a molecular-beam-epitaxy method, and the excessive amount of V group atom may be easily controlled by setup of growth temperature. The above-mentioned compound semiconductor substrate (1) will be easily manufactured by enforcing the manufacture approach (2) of the compound semiconductor substrate of the above-mentioned configuration.

[0016] Moreover, by the manufacture approach (3) of the above-mentioned compound semiconductor substrate, said V group atom is included superfluously. A still larger sludge than that of said V group atom can be formed into a group-III-V-semiconducter layer, consequently propagation of a rearrangement is prevented further, and it describes above. Dislocation density [/ near the group-III-V-semiconducter layer front face] can manufacture the compound semiconductor substrate reduced further.

[0017]

[Working Example(s) and Comparative Example(s)] Hereafter, the example of the compound semiconductor substrate concerning this invention and its manufacture approach is explained based on a drawing. Drawing 1 is the sectional view having shown typically the example 1 of the compound semiconductor substrate concerning this invention, and 11 in drawing shows Si substrate. On the Si substrate 11, the GaAs layer 12 whose thickness is about 1 micrometer is formed, and the GaAs layer 13 whose thickness which contains As in an excess about 0.4% is about 0.2 micrometers is formed on the GaAs layer 12. On the GaAs layer 13, the GaAs layer 14 whose thickness is about 2 micrometers is formed, and the compound semiconductor substrate 10 is constituted including these Si substrate 11, the GaAs layers 12 and 14, and the GaAs layer 13 that contains As superfluously.

[0018] When manufacturing the compound semiconductor substrate 10 of such a configuration, it is made to grow up by the molecular-beam-epitaxy method, using Solid-state As and Solid-state Ga as a source of vacuum evaporationo. First, after field bearing washes Si substrate which inclined in the [110] directions 2 degrees by about 1% of fluoric acid (HF), it inserts in a molecular beam epitaxy chamber, heats at about 900 degrees C, and carries out evaporation cleaning of the oxide film on Si substrate 11 front face in a field (001). Next, with a two-step grown method, first, about 20 and growth temperature are set as about 400 degrees C, a growth rate is set as about 0.3 micrometer/h for the molecular-beam

intensity ratio to Ga of As, respectively, and GaAs layer (initial layer) 12a whose thickness is about 100nm is grown up on the Si substrate 11. Next, about 20 and growth temperature are set as about 600 degrees C, a growth rate is set as about 1 micrometer/h for the molecular-beam intensity ratio to Ga of As, respectively, GaAs layer 12b whose thickness is about 900nm is grown up, and the GaAs layer 12 of about 1 micrometer of sum totals is formed. Next, about 20 and growth temperature are set as about 200 degrees C, a growth rate is set as about 1 micrometer/h for the molecular-beam intensity ratio to Ga of As, respectively, and epitaxial growth of the GaAs layer 13 whose thickness which contains As superfluously on the GaAs layer 12 is about 0.2 micrometers is carried out. Next, about 20 and growth temperature are set as about 600 degrees C, a growth rate is set as about 1 micrometer/h for the molecular-beam intensity ratio to Ga of As, respectively, and epitaxial growth of the GaAs layer 14 whose thickness is about 2 micrometers is carried out on the GaAs layer 13.

[0019] As a result of measuring the superfluous amount of As(es) in the GaAs layer 13 of the compound semiconductor substrate 10 manufactured by the above-mentioned approach, it was about 0.4%. In addition, this superfluous amount of As(es) was converted and calculated from the lattice constant of the GaAs layer 13 measured according to the X diffraction based on the relation (Thin Solid Films:231 (1993) 61-73 drawing 3 R> 3) between the superfluous amount of As(es) already calculated, and the elongation of a lattice constant.

[0020] Below, the result of having measured the dislocation density and carrier concentration of a compound semiconductor substrate concerning an example 1 is explained. Dislocation density dipped the sample in the melting potassium hydroxide (KOH) kept at about 350 degrees C for about 30 seconds, and asked for it from the number of pits per [which appeared in GaAs layer 14 front face] unit area. Moreover, it asked for carrier concentration by the capacity-amplitude measurement. In addition, that in which the GaAs layer 13 in the compound semiconductor substrate 10 is not formed as an example 1 of a comparison was used. Moreover, as an example 2 of a comparison, that in which the superlattice layer whose thickness is about 0.3 micrometers is inserted was used instead of the GaAs layer 13 in the compound semiconductor substrate 10. This superlattice layer grew up about 20nm In0.1 Ga0.9 As layer and about 10nm GaAs layer by turns by the molecular beam epitaxy, and carried out the laminating of the about ten layers of this, and the In0.1 Ga0.9 As layer grew up the molecular-beam intensity ratio to Ga of As by setting about 18 and growth temperature as about 550 degrees C, and setting a growth rate as about 1.1 micrometer/h. Moreover, as an example 3 of a comparison, that in which Si dope layer whose thickness is about 0.2 micrometers is inserted was used instead of the GaAs layer 13 in the compound semiconductor substrate 10. By the molecular beam epitaxy, this Si dope layer is 3 about 3x1020 pieces/cm in a GaAs layer. It was made to grow up including Si.

[0021] Drawing 2 is the graph which showed the measurement result of the dislocation density in the GaAs layer front face of the compound semiconductor substrate concerning an example 1 and the examples 1-3 of a comparison. The dislocation density of the compound semiconductor substrate 10 concerning an example 1 is abbreviation 5x106 cm-2, and although the example 1 of a comparison in which the GaAs layer 13 which contains As superfluously is not formed is started, it is decreasing compared with a case (about 3x107 cm- 2). moreover -- although the dislocation density of the compound semiconductor substrate 10 concerning an example 1 starts the example 2 of a comparison in which the superlattice layer was inserted -- a case (about 4x106 cm- 2) and abbreviation -- it was comparable, and although the example 3 of a comparison was started, it was larger than the case a little.

[0022] Moreover, drawing 3 is the curvilinear Fig. having shown the relation between concentration of electrons and the distance from a compound semiconductor substrate front face, and in the case of the thing concerning an example 1, (a) shows the case, although (b) starts the example 3 of a comparison. Separation between the transistor components which a case shows n mold although an example 1 is started so that clearly from drawing 3 , the part of the GaAs layer 13 which contains As superfluously has three or less [1013cm -] low concentration of electrons (high resistance), therefore were formed in the GaAs layer 14 can be performed easily. On the other hand, although the example 3 of a comparison was started, as for the case, it turned out that n mold as a result of spreading Si in said Si dope layer even in a surface layer is shown, and it is easy to have a bad influence on the GaAs layer which performs

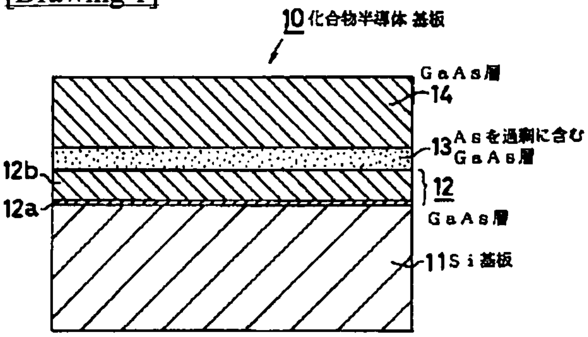
component formation.
[0023] In the compound semiconductor substrate 10 concerning an example 1, some As atoms can be condensed and deposited in the GaAs layer 13 which contains As atomic number in an excess about 0.4%, and pinning of the rearrangement produced by this condensation and As particle which deposited in the interface with the GaAs layer 12 which carried out epitaxial growth to the Si substrate 11 can be carried out so that clearly from these results. For this reason, by the GaAs layer 13 which contains As atom superfluously, propagation of the rearrangement to GaAs layer 14 front face can be blocked, consequently dislocation density [/ near the GaAs layer 14 front face] can be reduced. Moreover, since any atoms other than a configuration element are not included in the GaAs layer 13 which contains As atom superfluously, there is also little effect affect the band structure of the GaAs layer 14, and the compound semiconductor substrate of the high quality excellent in electrical characteristics also with little change of carrier concentration can be obtained.
[0024] Moreover, the process which makes As atom incorporate superfluously can be easily carried out by adopting a molecular-beam-epitaxy method, and the excessive amount of As atom can be easily controlled by the manufacture approach of the compound semiconductor substrate 10 concerning an example 1 by setup of growth temperature. Therefore, the compound semiconductor substrate 10 can be easily manufactured by enforcing this manufacture approach.
[0025] Next, the compound semiconductor substrate concerning examples 2-7 has the same configuration as the compound semiconductor substrate 10 and abbreviation concerning the example 1 shown in drawing 1 . However, in case epitaxial growth of the GaAs layer 13 which contains As superfluously is carried out, the point that the superfluous amount of As(es) is migrating to about 0.2 to about 1.5% of range is different from the thing concerning an example 1 by changing growth temperature from 180 degrees C of abbreviation to 250 degrees C of abbreviation. Below, the result of having measured the dislocation density of GaAs layer 14 front face in the compound semiconductor substrate concerning examples 2-7 is explained. In addition, as an example of a comparison, what contained As atom in the excess about 0.1% was manufactured collectively.
[0026] In the case of the examples 2-7 which contain As atom superfluously in about 0.2 to about 1.5% of range, dislocation density was low, although dislocation density was as high as abbreviation 2x106 cm-2 when the superfluous amount of As(es) was the example of a comparison which is 0.1% so that clearly [drawing 4 / drawing 4 may be the curvilinear Fig. having shown the relation between dislocation density and the superfluous amount of As(es) and] from this drawing.
[0027] Next, the compound semiconductor substrate concerning an example 8 has the same configuration as the compound semiconductor substrate 10 and abbreviation concerning the example 1 shown in drawing 1 . However, before carrying out epitaxial growth of the GaAs layer 13 and growing up the GaAs layer 14 succeedingly after that, the heat treatment process for about 10 minutes (a temperature rise and the fall time are not included) was given at about 700 degrees C higher than the growth temperature of the GaAs layer 14. Drawing 5 is drawing having shown the heat pattern of the compound semiconductor substrate concerning an example 8. The flux of As was irradiated in order to protect that As evaporates from GaAs layer 13 front face in the case of this heat treatment.
[0028] As a result of measuring the dislocation density in the compound semiconductor substrate front face concerning the example 8 which performed this heat treatment, as compared with 5x106 cm-2 of the thing of the example 1 which does not heat-treat, it decreased even to 2x106 cm-2.
[0029] With the compound semiconductor substrate concerning an example 8, while the same effectiveness as the case of an example 1 is acquired, some As atoms can be made to be able to condense further in the GaAs layer 13 which contains As atom superfluously, and a large sludge can be deposited, the propagation prevention effectiveness of a rearrangement can be heightened further, therefore dislocation density [/ near the GaAs layer 14 front face] can be further reduced, so that clearly from the above-mentioned result. Moreover, this heat treatment temperature could be set up lower than the temperature shown in reference (61 application physics No. 2, pp 126-133, and 1992), and was able to aim at compaction of growth time amount, and saving of heater power.
[0030] In addition, although the above-mentioned example explained the case where the GaAs layer 12

and the GaAs layer 13 which contains As superfluously among 14 were made to carry out epitaxial growth for each In the another example, it is [layer / a GaP layer, / InGaAs] another instead of the GaAs layers 12 and 14. While a group-III-V-semiconducter layer is made to carry out epitaxial growth It is [layer / the GaAs layer 13 which contains As superfluously / the GaP layer which contains V group atoms, such as P and As, superfluously instead of, an InGaAs layer, etc.] another. A group-III-V-semiconducter layer may be made to carry out epitaxial growth.
[0031] Moreover, although the thing of the above-mentioned example explained the case where the one-layer GaAs layer 13 was made to carry out epitaxial growth for each, in the another example, this may be more than two-layer.
[0032]
[Effect of the Invention] If it is in the compound semiconductor substrate (1) concerning this invention as explained in full detail above it consists of the same configuration element as group-III-V-semiconducter layer -- compared with an III group atom, V group atom is superfluously included in 1.5% or less of range 0.2% or more Since at least one or more layers of group-III-V-semiconducter layers are included Above Compared with an III group atom, said V group atom is superfluously included in 1.5% or less of range 0.2% or more. Said some of V group atoms can be condensed and deposited in a group-III-V-semiconducter layer. By this condensation and V group atom particle which deposited The above which carried out epitaxial growth on Si substrate and this Si substrate Pinning of the rearrangement produced in the interface with a group-III-V-semiconducter layer can be carried out. For this reason, said V group atom is included superfluously. It describes above by the group-III-V-semiconducter layer. Propagation of the rearrangement to a group-III-V-semiconducter layer front face can be blocked, consequently it describes above. Dislocation density [/ near the group-III-V-semiconducter layer front face] can be reduced. Moreover, said V group atom is included superfluously. Since any atoms other than a configuration element are not included in a group-III-V-semiconducter layer, it describes above. While being able to lessen effect affect the band structure of a group-III-V-semiconducter layer, the compound semiconductor substrate of the high quality which could also lessen change of carrier concentration, therefore was excellent in electrical characteristics can be obtained.
[0033] Moreover, if it is in the manufacture approach (2) of a compound semiconductor substrate V group atom is made to incorporate superfluously in 1.5% or less of range 0.2% or more compared with III group atom, and V group atom is included superfluously. Since at least one or more layers of group-III-V-semiconducter layers are grown up The process which makes said V group atom incorporate superfluously can be easily carried out by adopting the molecule epitaxy method, and the excessive amount of said V group atom can be easily controlled by setup of growth temperature. Therefore, by enforcing this manufacture approach, the above-mentioned compound semiconductor substrate (1) can be manufactured easily.
[0034] Moreover, if it is in the manufacture approach (3) of a compound semiconductor substrate Compared with III group atom, V group atom is included superfluously. After carrying out epitaxial growth of the group-III-V-semiconducter layer, it is made to grow up after that. Since the heat treatment process in temperature higher than the growth temperature of a group-III-V-semiconducter layer is given Said V group atom is included superfluously. A still larger sludge than that of said V group atom can be formed into a group-III-V-semiconducter layer. Consequently, propagation of a rearrangement can be prevented further and described above. Dislocation density [/ near the group-III-V-semiconducter layer front face] can manufacture the compound semiconductor substrate reduced further.

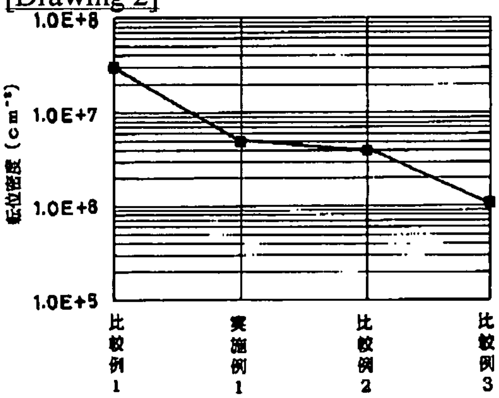
[Translation done.]

DRAWINGS

[Drawing 1]

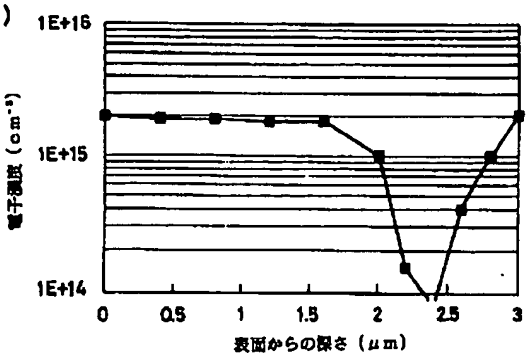


[Drawing 2]



[Drawing 3]

(a)



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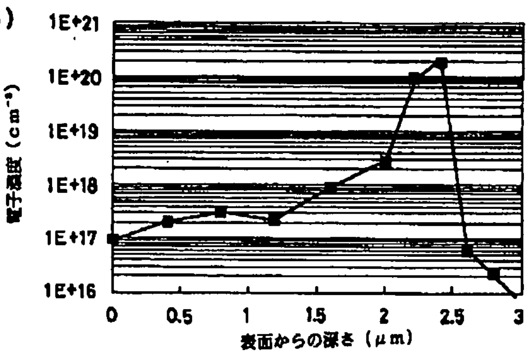
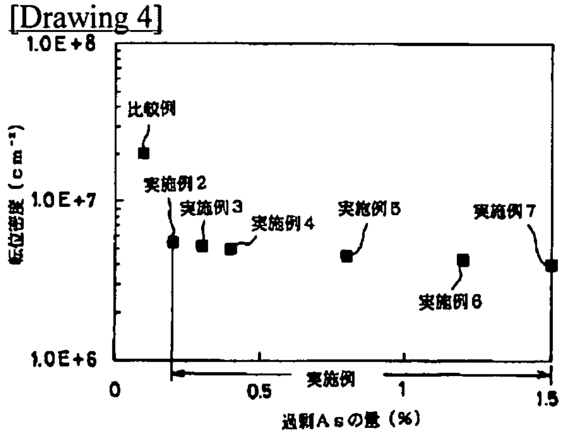
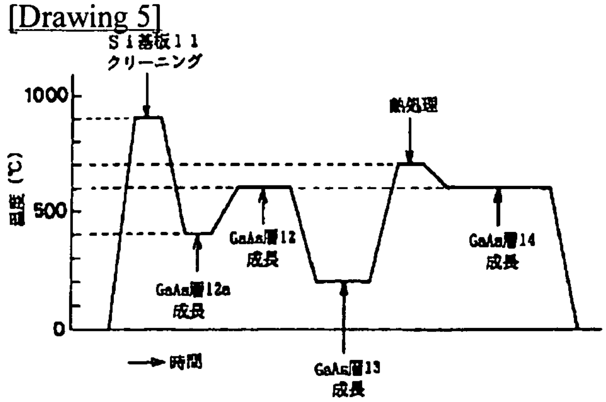


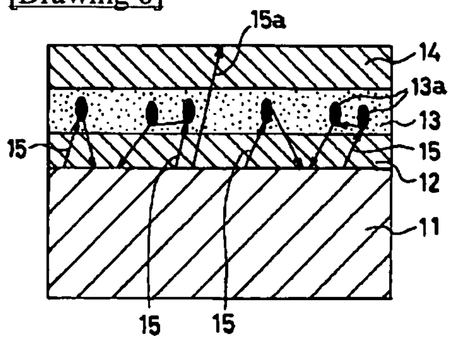
[Drawing 4]



[Drawing 5]



[Drawing 6]



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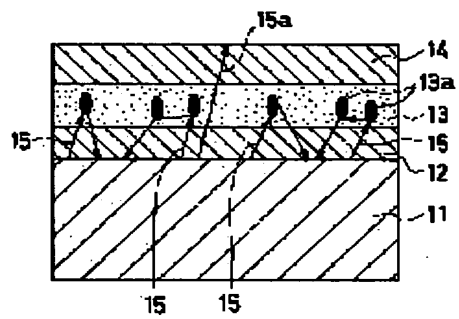
(54) COMPOUND SEMICONDUCTOR SUBSTRATE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To lessen the dislocation density and also, lessen the band structure and the change of carrier concentration by providing a III-V compound semiconductor 9 layer which contains group V atoms excessively within the specified range as compared with group III atoms by at least one layer or more.
CONSTITUTION: A GaAs layer 12 epitaxially grown is made on an Si substrate 11. And, a GaAs layer 13 containing excessive As is made on the GaAs layer 12. During the growth, since the release of As from the surface of the GaAs layer 13 is suppressed, stoichimetically excessive As is taken into the GaAs layer 13. The content of excessive As within the GaAs layer 13 for reducing the density of dislocation 15a should be 0.2% or more, while the upper limit value is limited by growth method, so in molecular beam epitaxial growth method, 1.5% becomes the upper limit value.



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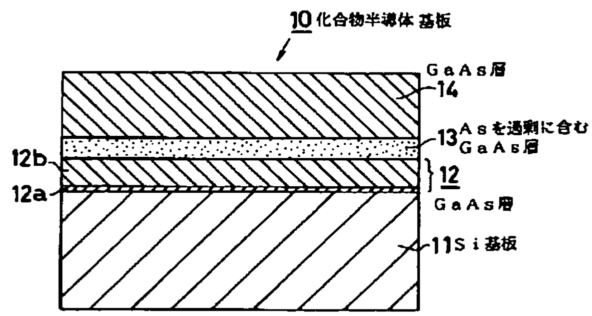
(54)【発明の名称】　化合物半導体基板及びその製造方法

(57)【要約】

【構成】　ＧａＡｓ層１２、１４と同一の構成元素から成り、Ｇａ原子に比べてＡｓ原子を０．２％以上１．５％以下の範囲で過剰に含むＧａＡｓ層１３を１層含んでいる化合物半導体基板１０。

【効果】　ＧａＡｓ層１３中にＡｓ原子の一部を析出させることができ、この析出したＡｓ粒子により、Ｓｉ基板１１とＧａＡｓ層１２との界面に生じた転位をピンニングさせることができるため、転位の伝播をブロックすることができ、ＧａＡｓ層１４表面近傍における転位密度を低減することができる。またＧａＡｓ層１３には構成元素以外の原子を含んでいないため、ＧａＡｓ層１４のバンド構造に及ぼす影響も少なく、キャリア濃度の変化も少ない、電気的特性に優れた高品質の化合物半導体基板１０を得ることができる。



【特許請求の範囲】

【請求項1】　シリコン基板上に III－V族化合物半導体層がエピタキシャル成長させられた化合物半導体基板において、前記 III－V族化合物半導体層と同一の構成元素から成り、 III族原子に比べてV族原子を0．2％以上1．5％以下の範囲で過剰に含む III－V族化合物半導体層を少なくとも1層以上含んでいることを特徴とする化合物半導体基板。

【請求項2】　シリコン基板上に III－V族化合物半導体層をエピタキシャル成長させる化合物半導体基板の製造方法において、 III族原子に比べてV族原子を0．2％以上1．5％以下の範囲で過剰に取り込ませ、V族原子を過剰に含む III－V族化合物半導体層を成長させる工程を含むことを特徴とする化合物半導体基板の製造方法。

【請求項3】　III族原子に比べてV族原子を過剰に含む III－V族化合物半導体層をエピタキシャル成長させた後、その後に成長させる III－V族化合物半導体層の成長温度よりも高い温度での熱処理工程を施すことを特徴とする請求項2記載の化合物半導体基板の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は化合物半導体基板及びその製造方法に関し、より詳細には、例えば光または高速電子デバイス等に使用される化合物半導体基板及びその製造方法に関する。

【0002】

【従来の技術】近年、基板上にこれとは異種の化合物半導体をエピタキシャル成長させ、前記基板及び化合物半導体におけるそれぞれの長所を活用可能な化合物半導体基板が研究されている。例えばシリコン（以下、Ｓｉと記す）基板上にＧａＡｓをエピタキシャル成長させることにより、Ｓｉが保有する機械的強度と、ＧａＡｓが保有する高速応答性とを兼ね備えた化合物半導体基板が作製されており、このような方法によって得られた化合物半導体基板は電子デバイス、光デバイス等に応用されている。しかしＳｉとＧａＡｓとにおける格子定数及び熱膨張係数には大きな差があり、この格子定数差に起因してＳｉ基板とＧａＡｓ層との界面に転位が形成され易く、また前記熱膨張係数差に基づいて発生した応力により前記転位が前記ＧａＡｓ層の表面に向かって伝播し易い。この結果、前記ＧａＡｓ層表面には前記転位が多く存在し、前記ＧａＡｓ層における表面近傍の結晶性が低下し、デバイス等としての機能を良好に発揮させることが難しいという問題があった。

【0003】ＧａＡｓ層表面近傍における転位密度を低減する方法として、前記ＧａＡｓ層中に転位の伝播を抑制するための転位低減層を挿入することが試みられている。この転位低減層にはＧａＡｓ層とは異なる組成を有する歪超格子層や、不純物が添加された層等が検討されている（応用物理：６１巻２号、pp126-133、1992 ）。

【0004】前記歪超格子層には、例えばＩｎＧａＡｓ層やＧａＡｓＰ層等のようなＧａＡｓ層とは格子定数が異なる化合物が用いられており、この歪み超格子層が挿入されると、これから生じた歪で前記転位の伝播方向が曲げられ、該転位の伝播が抑えられることにより、前記ＧａＡｓ層表面近傍における転位密度の低減が図られる。またＧａＡｓ層中に例えばＺｎ、Ｉｎ、Ｓｉ原子等の不純物が添加されると、結晶が硬くなる効果と前記転位がピンニングされる効果とにより、前記ＧａＡｓ層表面近傍への転位の伝播が抑制され、転位密度の低減が図られる。

【0005】

【発明が解決しようとする課題】しかしながら上記した歪超格子層が挿入された化合物半導体基板においては、前記歪超格子層によりＧａＡｓ層のバンド構造が変化し易く、このバンド構造の変化がＧａＡｓ層表面近傍の電気的特性に悪影響を及ぼし易いという課題があった。

【0006】また前記不純物が添加された化合物半導体基板においては、前記不純物が前記転位低減層からＧａＡｓ層表面近傍に拡散してしまうと、Ｚｎ、ＩｎまたはＳｉ原子等の不純物がドーパントとして作用し、ＧａＡｓ層表面近傍におけるキャリア濃度に変化が生じて電気的特性に悪影響を及ぼし易いという課題があった。

【0007】本発明はこのような課題に鑑みなされたものであり、Ｓｉ基板上に III－V族化合物半導体層がエピタキシャル成長させられた化合物半導体基板表面近傍における転位密度が少なく、バンド構造やキャリア濃度の変化も少ない、電気的特性に優れた高品質の化合物半導体基板及びその製造方法を提供することを目的としている。

【0008】

【課題を解決するための手段】上記目的を達成するために本発明に係る化合物半導体基板は、シリコン基板上に III－V族化合物半導体層がエピタキシャル成長させられた化合物半導体基板において、前記 III－V族化合物半導体層と同一の構成元素から成り、 III族原子に比べてV族原子を0．2％以上1．5％以下の範囲で過剰に含む III－V族化合物半導体層を少なくとも1層以上含んでいることを特徴としている（1）。

【0009】また本発明に係る化合物半導体基板の製造方法は、シリコン基板上に III－V族化合物半導体層をエピタキシャル成長させる化合物半導体基板の製造方法において、 III族原子に比べてV族原子を0．2％以上1．5％以下の範囲で過剰に取り込ませ、V族原子を過剰に含む III－V族化合物半導体層を成長させる工程を含むことを特徴としている（2）。

【0010】また本発明に係る化合物半導体基板の製造方法は、上記（2）記載の化合物半導体基板の製造方法により、 III族原子に比べてV族原子を過剰に含む III

－Ｖ族化合物半導体層をエピタキシャル成長させた後、その後に成長させる III－Ｖ族化合物半導体層の成長温度よりも高い温度での熱処理工程を施すことを特徴としている（3）。

【0011】

【作用】例えばＧａＡｓ（ III－Ｖ族化合物）層の場合、分子線エピタキシ法を用いて比較的低温（２００～３００℃）の所定温度で成長させることにより、Ｇａ（Ｖ族原子）に比べて過剰な所定濃度のＡｓ（ III族原子）を含むＧａＡｓ層をエピタキシャル成長させ得ることが知られている (Thin Solid Films:231(1993)61-73)。この場合、主として成長温度を変えることにより、前記ＧａＡｓ層中におけるＡｓの過剰含有濃度を制御している。

【0012】図6はＳｉ基板上にＧａＡｓ層がエピタキシャル成長させられ、このＧａＡｓ層中にＡｓを過剰に含むＧａＡｓ層を１層含んでいる化合物半導体基板における転位の伝播を説明するために示した模式的断面図であり、図中１１はＳｉ基板を示している。Ｓｉ基板１１上にはエピタキシャル成長させられたＧａＡｓ層１２が形成され、ＧａＡｓ層１２上には過剰のＡｓを含有するＧａＡｓ層１３が形成されている。ＧａＡｓ層１３は上記した分子線エピタキシ法を用いて比較的低温の所定温度で成長させられており、成長の際、ＧａＡｓ層１３表面からのＡｓの離脱が抑制されるため、ＧａＡｓ層１３中には化学量論的に過剰のＡｓが取り込まれている。またＧａＡｓ層１３上にはＧａＡｓ層１２と略同様にエピタキシャル成長させられたＧａＡｓ層１４が形成されており、ＧａＡｓ層１４のエピタキシャル成長工程中において、ＧａＡｓ層１３中に過剰に取り込まれたＡｓの一部が凝集し、金属Ａｓ１３ａとして析出することとなる。

【0013】このように構成された化合物半導体基板では、Ｓｉ基板１１とＧａＡｓ層１２との界面に発生した転位１５が金属Ａｓ１３ａによりピンニングされることとなる。したがって一部の転位１５ａを除き、ほとんどの転位１５がＧａＡｓ層１３によりブロックされてＧａＡｓ層１４への伝播が阻止されることとなり、この結果、ＧａＡｓ層１４表面近傍における転位１５ａの密度が減少する。転位１５ａの密度を減少させるためのＧａＡｓ層１３中における過剰なＡｓの含有量は０．２％以上が必要となる一方、上限値は成長法により制約されることとなり、分子線エピタキシャル成長法においては１．５％が上限値となる。

【0014】上記構成の化合物半導体基板（1）によれば、前記 III族原子に比べて前記Ｖ族原子を０．２％以上１．５％以下の範囲で過剰に含む III－Ｖ族化合物半導体層中に前記Ｖ族原子の一部を凝集・析出させ得ることとなり、該凝集・析出したＶ族原子粒子により、Ｓｉ基板と該Ｓｉ基板上にエピタキシャル成長させられた前記 III－Ｖ族化合物半導体層との界面に生じた転位をピンニングさせ得ることとなる。このため、前記Ｖ族原子を過剰に含む III－Ｖ族化合物半導体層により、前記 III－Ｖ族化合物半導体層表面への転位の伝播をブロックし得ることとなり、この結果、前記 III－Ｖ族化合物半導体層表面近傍における転位密度を低減し得ることとなる。また前記Ｖ族原子を過剰に含む III－Ｖ族化合物半導体層には化合物半導体層の構成元素以外の原子を含んでいないため、前記 III－Ｖ族化合物半導体層のバンド構造に及ぼす影響を少なくし得ると共に、キャリア濃度の変化も少なくし得ることとなり、したがって電気的特性に優れた高品質の化合物半導体基板が得られることとなる。

【0015】また上記構成の化合物半導体基板の製造方法（2）におけるＶ族原子を過剰に取り込ませる工程は、分子線エピタキシ法を採用することにより容易に実施され、またＶ族原子の過剰量は成長温度の設定により容易に制御され得る。上記構成の化合物半導体基板の製造方法（2）を実施することにより上記化合物半導体基板（1）が容易に製造されることとなる。

【0016】また上記した化合物半導体基板の製造方法（3）により、前記Ｖ族原子を過剰に含む III－Ｖ族化合物半導体層中に前記Ｖ族原子のより一層大きい析出物を形成し得ることとなり、この結果、転位の伝播がより一層防止され、前記 III－Ｖ族化合物半導体層表面近傍における転位密度がより一層低減された化合物半導体基板を製造し得ることとなる。

【0017】

【実施例及び比較例】以下、本発明に係る化合物半導体基板及びその製造方法の実施例を図面に基づいて説明する。図１は本発明に係る化合物半導体基板の実施例１を模式的に示した断面図であり、図中１１はＳｉ基板を示している。Ｓｉ基板１１上には厚さが約１μmのＧａＡｓ層１２が形成され、ＧａＡｓ層１２上にはＡｓを約０．４％過剰に含む厚さが約０．２μmのＧａＡｓ層１３が形成されている。ＧａＡｓ層１３上には厚さが約２μmのＧａＡｓ層１４が形成されており、これらＳｉ基板１１、ＧａＡｓ層１２、１４、Ａｓを過剰に含むＧａＡｓ層１３を含んで化合物半導体基板１０が構成されている。

【0018】このような構成の化合物半導体基板１０を製造する場合、蒸着源として固体Ａｓ及び固体Ｇａを用い、分子線エピタキシ法により成長させる。まず、面方位が（００１）面で、［１１０］方向に2°傾いたＳｉ基板を約１％のフッ酸（ＨＦ）で洗浄した後、分子線エピタキシチャンバーに挿入し、約９００℃に加熱してＳｉ基板１１表面上の酸化膜を蒸発クリーニングする。次に二段階成長法により、まずＡｓのＧａに対する分子線強度比を約２０、成長温度を約４００℃、成長速度を約０．３μm／ｈにそれぞれ設定し、Ｓｉ基板１１上に厚

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さが約１００ｎｍのＧａＡｓ層（初期層）１２ａを成長させる。次にＡｓのＧａに対する分子線強度比を約２０、成長温度を約６００℃、成長速度を約１μｍ／ｈにそれぞれ設定し、厚さが約９００ｎｍのＧａＡｓ層１２ｂを成長させ、合計約１μｍのＧａＡｓ層１２を形成する。次にＡｓのＧａに対する分子線強度比を約２０、成長温度を約２００℃、成長速度を約１μｍ／ｈにそれぞれ設定し、ＧａＡｓ層１２上にＡｓを過剰に含む厚さが約０．２μｍのＧａＡｓ層１３をエピタキシャル成長させる。次にＡｓのＧａに対する分子線強度比を約２０、成長温度を約６００℃、成長速度を約１μｍ／ｈにそれぞれ設定し、ＧａＡｓ層１３上に厚さが約２μｍのＧａＡｓ層１４をエピタキシャル成長させる。

【００１９】上記の方法により製造された化合物半導体基板１０のＧａＡｓ層１３中における過剰のＡｓ量を測定した結果、約０．４％であった。なおこの過剰のＡｓ量は、すでに求められている過剰なＡｓ量と格子定数の伸びとの関係（Thin Solid Films:231(1993)61-73 図3）をもとに、Ｘ線回折により測定したＧａＡｓ層１３の格子定数から換算して求めた。

【００２０】以下に、実施例１に係る化合物半導体基板の転位密度及びキャリア濃度を測定した結果について説明する。転位密度は約３５０℃に保った溶融水酸化カリウム（ＫＯＨ）に試料を約３０秒間浸し、ＧａＡｓ層１４表面に現れた単位面積当たりのピット数から求めた。またキャリア濃度は容量－電圧測定により求めた。なお比較例１として、化合物半導体基板１０におけるＧａＡｓ層１３が形成されていないものを用いた。また比較例２として、化合物半導体基板１０におけるＧａＡｓ層１３の代わりに、厚さが約０．３μｍの超格子層が挿入されているものを用いた。この超格子層は、約２０ｎｍの$In_{0.1}Ga_{0.9}As$層と約１０ｎｍのＧａＡｓ層とを分子線エピタキシャル法により交互に成長させ、これを１０層ほど積層したものであり、$In_{0.1}Ga_{0.9}As$層はＡｓのＧａに対する分子線強度比を約１８、成長温度を約５５０℃、成長速度を約１．１μｍ／ｈに設定することにより成長させた。また比較例３として、化合物半導体基板１０におけるＧａＡｓ層１３の代わりに、厚さが約０．２μｍのＳｉドープ層が挿入されているものを用いた。このＳｉドープ層は分子線エピタキシャル法により、ＧａＡｓ層中に約3×10^{20}個／cm^3のＳｉを含んで成長させた。

【００２１】図２は実施例１及び比較例１～３に係る化合物半導体基板のＧａＡｓ層表面における転位密度の測定結果を示したグラフである。実施例１に係る化合物半導体基板１０の転位密度は約5×10^6 cm^{-2}であり、Ａｓを過剰に含むＧａＡｓ層１３が形成されていない比較例１に係るものの場合（約3×10^7 cm^{-2}）に比べて減少している。また実施例１に係る化合物半導体基板１０の転位密度は超格子層が挿入された比較例２に係るものの場合（約4×10^6 cm^{-2}）と略同程度であり、また比較例３に係るものの場合よりは幾分大きかった。

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【００２２】また図３は電子濃度と化合物半導体基板表面からの距離との関係を示した曲線図であり、（ａ）は実施例１に係るものの場合、（ｂ）は比較例３に係るものの場合を示している。図３から明らかなように、実施例１に係るものの場合はｎ型を示し、Ａｓを過剰に含むＧａＡｓ層１３の部分は10^{13} cm^{-3}以下の低い電子濃度（高抵抗）になっており、したがってＧａＡｓ層１４に形成されたトランジスタ素子間の分離を容易に行える。一方比較例３に係るものの場合は前記Ｓｉドープ層中のＳｉが表面層にまで拡散した結果ｎ型を示し、素子形成を行うＧａＡｓ層に悪影響を及ぼし易いことが分かった。

【００２３】これらの結果から明らかなように、実施例１に係る化合物半導体基板１０では、Ａｓ原子数を約０．４％過剰に含むＧａＡｓ層１３中にＡｓ原子の一部を凝集・析出させることができ、この凝集・析出したＡｓ粒子により、Ｓｉ基板１１とエピタキシャル成長させたＧａＡｓ層１２との界面に生じた転位をピンニングさせることができる。このため、Ａｓ原子を過剰に含むＧａＡｓ層１３により、ＧａＡｓ層１４表面への転位の伝播をブロックすることができ、この結果、ＧａＡｓ層１４表面近傍における転位密度を低減することができる。またＡｓ原子を過剰に含むＧａＡｓ層１３には構成元素以外の原子を含んでいないため、ＧａＡｓ層１４のバンド構造に及ぼす影響も少なく、キャリア濃度の変化も少ない、電気的特性に優れた高品質の化合物半導体基板を得ることができる。

【００２４】また実施例１に係る化合物半導体基板１０の製造方法では、Ａｓ原子を過剰に取り込ませる工程は分子線エピタキシ法を採用することにより容易に実施することができ、またＡｓ原子の過剰量は成長温度の設定により容易に制御することができる。したがってこの製造方法を実施することにより化合物半導体基板１０を容易に製造することができる。

【００２５】次に実施例２～７に係る化合物半導体基板は、図１に示した実施例１に係る化合物半導体基板１０と略同様の構成を有している。しかし、Ａｓを過剰に含むＧａＡｓ層１３をエピタキシャル成長させる際、成長温度を略１８０℃から略２５０℃まで変化させることにより、過剰のＡｓ量が約０．２％から約１．５％の範囲にわたっている点が実施例１に係るものと相違している。以下に、実施例２～７に係る化合物半導体基板におけるＧａＡｓ層１４表面の転位密度を測定した結果について説明する。なお比較例として、Ａｓ原子を約０．１％過剰に含んだものを併せて製造した。

【００２６】図４は転位密度と過剰のＡｓ量との関係を示した曲線図であり、この図から明らかなように、過剰なＡｓ量が０．１％の比較例の場合は転位密度が約２×

10^6 cm^{-2}と高かったが、As原子を約0．2％から約1．5％の範囲で過剰に含む実施例2～7の場合は転位密度が低かった。

【0027】次に実施例8に係る化合物半導体基板は、図1に示した実施例1に係る化合物半導体基板10と略同様の構成を有している。しかし、GaAs層13をエピタキシャル成長させ、その後引き続きGaAs層14を成長させる前に、GaAs層14の成長温度よりも高い約700℃で約10分間（温度上昇及び下降時間は含まず）の熱処理工程を施しておいた。図5は実施例8に係る化合物半導体基板のヒートパターンを示した図である。この熱処理の際、GaAs層13表面からAsが蒸発するのを防ぐため、Asのフラックスを照射した。

【0028】この熱処理を施した実施例8に係る化合物半導体基板表面における転位密度を測定した結果、熱処理を施さない実施例1のものの5×10^6 cm^{-2}に比較し、2×10^6 cm^{-2}にまで減少した。

【0029】上記結果から明らかなように、実施例8に係る化合物半導体基板では、実施例1の場合と同様の効果が得られると共に、As原子を過剰に含むGaAs層13中にAs原子の一部をより一層凝集させ、大きい析出物を析出させることができ、この結果、転位の伝播防止効果を一層高めることができ、したがってGaAs層14表面近傍における転位密度を一層低減することができる。またこの熱処理温度は文献（応用物理61巻2号、pp126-133, 1992 ）に示されている温度よりも低く設定することができ、成長時間の短縮や、ヒーターパワーの節約を図ることができた。

【0030】なお上記した実施例では、いずれもGaAs層12、14間にAsを過剰に含むGaAs層13がエピタキシャル成長させられた場合について説明したが、別の実施例ではGaAs層12、14の代わりにGaP層やInGaAs層等の別の III－V族化合物半導体層がエピタキシャル成長させられるとともに、Asを過剰に含むGaAs層13の代わりにPやAs等のV族原子を過剰に含むGaP層やInGaAs層等の別の III－V族化合物半導体層がエピタキシャル成長させられたものであってもよい。

【0031】また上記した実施例のものでは、いずれも1層のGaAs層13がエピタキシャル成長させられた場合について説明したが、別の実施例ではこれが2層以上であってもよい。

【0032】

【発明の効果】以上詳述したように本発明に係る化合物半導体基板（1）にあっては、 III－V族化合物半導体層と同一の構成元素から成り、 III族原子に比べてV族原子を0．2％以上1．5％以下の範囲で過剰に含む III－V族化合物半導体層を少なくとも1層以上含んでいるので、前記 III族原子に比べて前記V族原子を0．2％以上1．5％以下の範囲で過剰に含む III－V族化合物半導体層中に前記V族原子の一部を凝集・析出させることができ、該凝集・析出したV族原子粒子により、Si基板と該Si基板上にエピタキシャル成長させた前記 III－V族化合物半導体層との界面に生じた転位をピンニングさせることができる。このため、前記V族原子を過剰に含む III－V族化合物半導体層により、前記 III－V族化合物半導体層表面への転位の伝播をブロックすることができ、この結果、前記 III－V族化合物半導体層表面近傍における転位密度を低減することができる。また前記V族原子を過剰に含む III－V族化合物半導体層には構成元素以外の原子を含んでいないため、前記 III－V族化合物半導体層のバンド構造に及ぼす影響を少なくすることができると共に、キャリア濃度の変化も少なくすることができ、したがって電気的特性に優れた高品質の化合物半導体基板を得ることができる。

【0033】また化合物半導体基板の製造方法（2）にあっては、 III族原子に比べてV族原子を0．2％以上1．5％以下の範囲で過剰に取り込ませ、V族原子を過剰に含む III－V族化合物半導体層を少なくとも1層以上成長させるので、前記V族原子を過剰に取り込ませる工程は、分子エピタキシ法を採用することにより容易に実施することができ、また前記V族原子の過剰量は成長温度の設定により容易に制御することができる。したがってこの製造方法を実施することにより、上記化合物半導体基板（1）を容易に製造することができる。

【0034】また化合物半導体基板の製造方法（3）にあっては、 III族原子に比べてV族原子を過剰に含む III－V族化合物半導体層をエピタキシャル成長させた後、その後に成長させる III－V族化合物半導体層の成長温度よりも高い温度での熱処理工程を施しておくので、前記V族原子を過剰に含む III－V族化合物半導体層中に前記V族原子のより一層大きい析出物を形成することができ、この結果、転位の伝播をより一層防止することができ、前記 III－V族化合物半導体層表面近傍における転位密度がより一層低減された化合物半導体基板を製造することができる。

【図面の簡単な説明】

【図1】本発明に係る化合物半導体基板の実施例1を模式的に示した断面図である。

【図2】実施例1及び比較例1～3に係る化合物半導体基板のGaAs層表面における転位密度の測定結果を示したグラフである。

【図3】キャリア濃度と化合物半導体基板表面からの距離との関係を示した曲線図であり、（a）は実施例1のものの場合、（b）は比較例3のものの場合を示している。

【図4】転位密度と実施例2～7及び比較例に係る化合物半導体基板の含有する過剰のAs量との関係を示した曲線図である。

【図5】実施例8に係る化合物半導体基板のヒートパタ

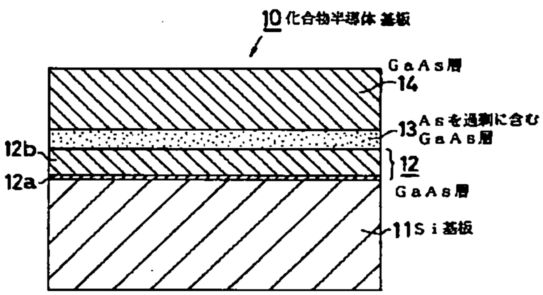
ーンを示した図である。

【図6】Ｓｉ基板上にＧａＡｓ層がエピタキシャル成長させられ、このＧａＡｓ層中にＡｓを過剰に含むＧａＡｓ層を１層含んでいる化合物半導体基板における転位の伝播を説明するために示した模式的断面図である。

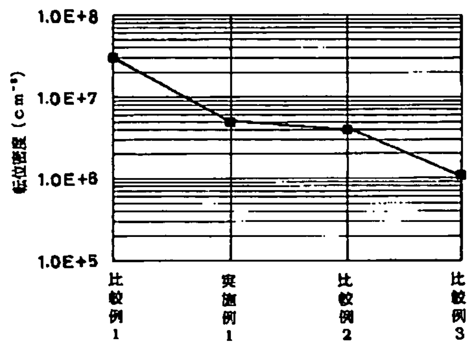
【符号の説明】

１０　化合物半導体基板
１１　シリコン基板
１２　ＧａＡｓ層
１３　Ａｓを過剰に含むＧａＡｓ層
１４　ＧａＡｓ層

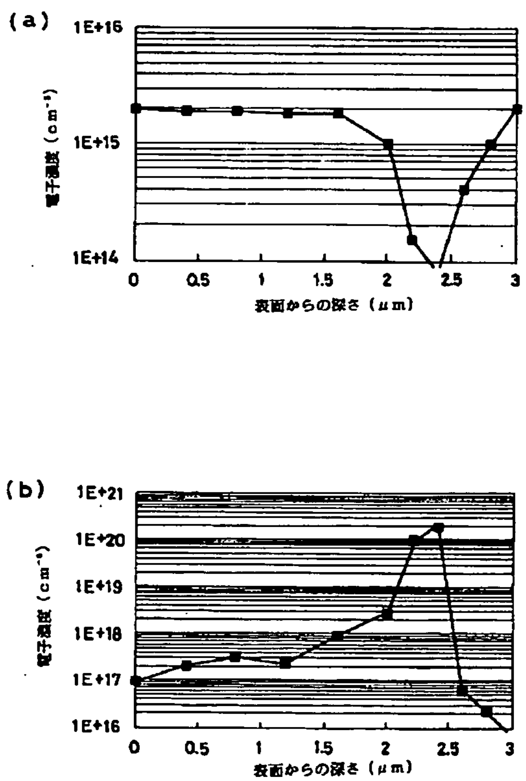
【図１】



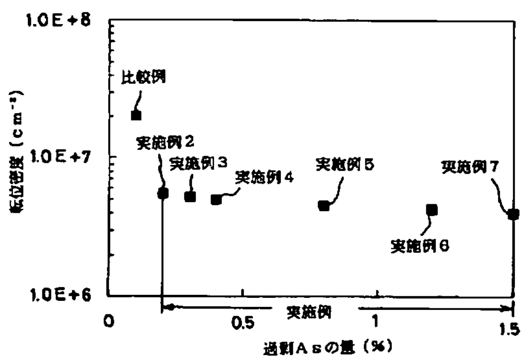
【図２】



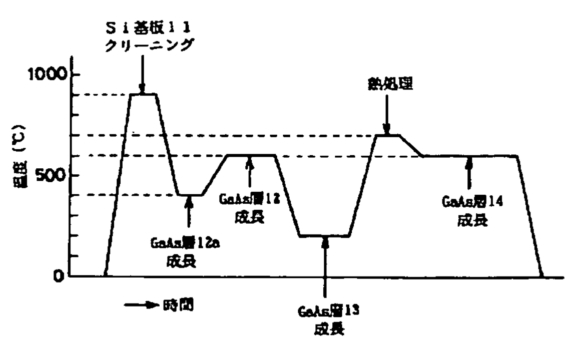
【図３】



【図４】



【図５】



【図6】